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MODEL 420

TOM
DIGITAL DRUM MACHINE

TECHNICAL MANUAL

by Rick Davies
and Stanley Jungleib

SEQUENTIAL/EUROPE
Postbus 16
3640 AA Mijdrecht
Netherlands

02979-6211
TELEX: 12721 SQNTL NL

SEQUENTIAL/U.S.A.
3051 North First Street
San Jose, CA 95134-2093
U.S.A.

(408) 946-5240
TELEX: 4997150 SEQCIR

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The Model 420 TOM Design Team:

PROJECT MANAGER/ENGINEER:	Tony Dean
FIRMWARE:	Bill Aspromonte
MIDI FIRMWARE:	Chris Meyer
DIGITAL SAMPLING SYSTEM DESIGN:	Paul Rutigliano
MECHANICAL ENGINEER:	Tom Benningfield
PC LAYOUT:	Jeff Oglevee
PRODUCT SUPPORT ENGINEER:	Scott Peterson

TABLE OF CONTENTS

SECTION 0

SYSTEM/CHASSIS

ABNORMAL POWER-ON INDICATIONS

Normally, when power is first switched on, the right display reads "00", the left display is blank, and the PATTERN LED and top function LED are lit. Unless it is merely a power supply problem, if no LEDs light there probably is a computer failure. It may be best to first troubleshoot the reset circuit.

UPDATES

The following corrective updates are covered by warranty, and should be installed if a customer complains.

TOM1_5 Software Update

This update corrects a problem caused by changing the STACK setting. (In versions TOM1_1 through 1_4, if STACK is adjusted while recording a pattern, other patterns recorded with one STACK setting are sometimes played back with the opposite setting, causing some patterns to sound considerably different.) To determine the software version installed without opening the 420, use the Memory Status function (see CM420). Order Sequential part #Z-1063 Software Update for the Model 420.

Cassette Interface

Add R183 (2.2M) to cassette interface circuit (see schematic A on page 1.3, and PARTS LIST/FUNCTIONAL DESCRIPTION for U128 on page 1.10, and for R183 on page 1.19). This improves tape storage and sync-to-tape operation. Serial numbers 001-170 and 351-806 do not have this mod, and should be updated.

Memory Loss

Early production models may suffer memory loss due to the reset circuit. All models with serial numbers over 1882 include a modification to the reset circuit which corrects this problem. If a customer complains of memory loss, take the following steps.

1. To check for presence of modification:

Disassemble the 420 (see page 0.5).

Check the printed circuit board for its revision (see Figure 0.1).

If board is "rev C," look for PCB 2 over the location of U153 (see Figure 0.1).

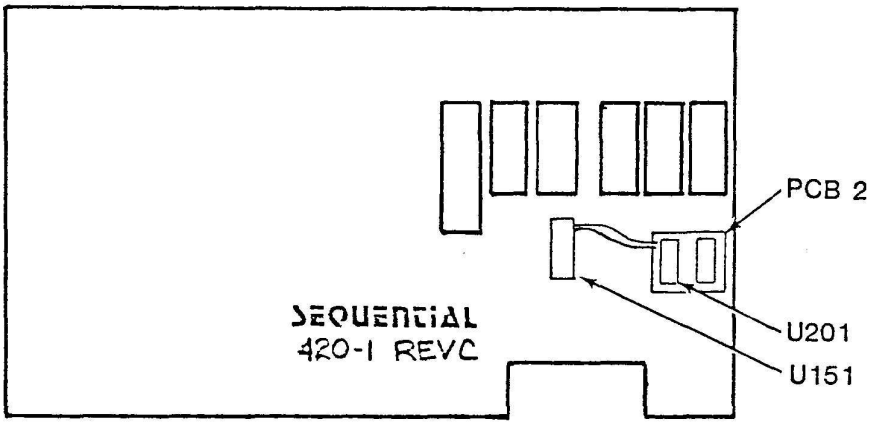


Figure 0.1
LOCATION OF RESET MODIFICATION

If the update is not present, order Sequential kit #UD0420-0.

2. To install the update:

Remove U153.

Place PCB2 in U153 location (orient as shown in Figure 0.1), then solder all pins.

Apply solder to the ends of the two wires from the update PCB, then connect the orange wire to U151 pin 14, and the violet wire to U151 pin 15.

3. For descriptions of the modified circuits, see PARTS LIST/FUNCTIONAL DESCRIPTION for U201, page 1.16.

4. Test the 420 for correct operation.

5. If the unit tests OK, reload the 420's patterns from tape.

6. To reassemble the 420, reverse the order of disassembly. (If the main PCB was removed, check that all washers are back in place.)

If the 420 is not modified, the following circuit descriptions and schematics apply:

U153-1, -4 ROM Decoder I-248 74HC02 quad NOR gate
See Figure 0.2. Since U144 software ROM represents a 16K block of memory, it is decoded separately by U153-4 from A14 and A15. (U153-1 inverts the chip select for correct polarity.)

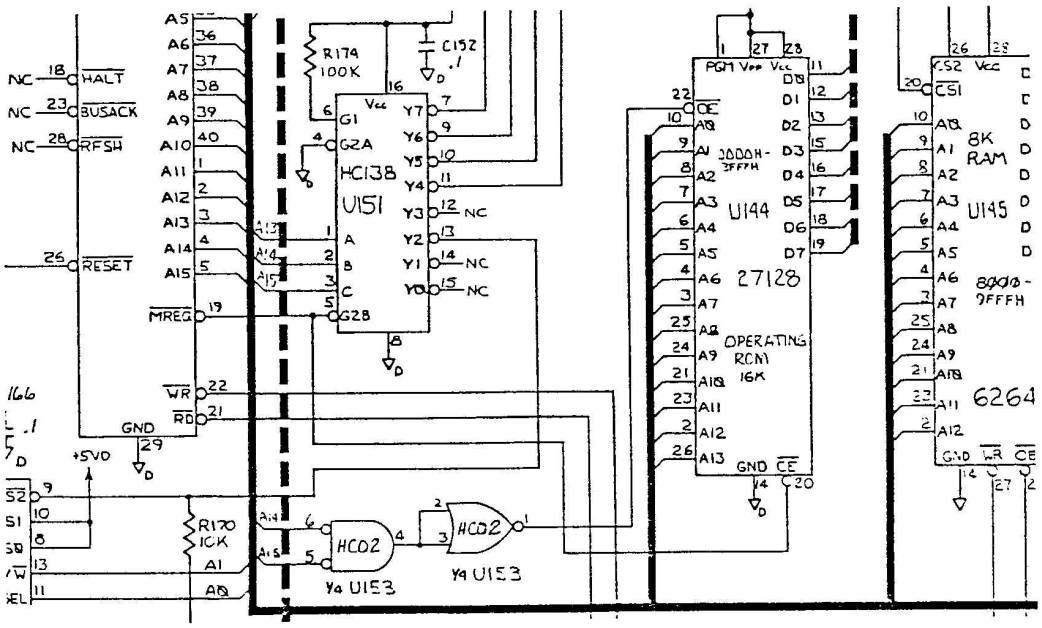


Figure 0.2
ORIGINAL ROM DECODING CIRCUIT

U153-13, -10 **Power Detect** I-248 **74HC02 quad NOR gate**

See Figure 0.3. Power is supplied to U153 by Vnv at pin -14. When power is off, pin -8 and -9 are held at Vnv by C156, ensuring that -RESET is low at power-up. When power is switched on, D129/R178/C155 generate unregulated dc at pin 12, bringing pin 13 low. Pin -9 goes low immediately, but R176/C156 delay the falling edge at pin 8, followed by -RESET going high. On power-off, pin-13 goes high, D132 bypasses R176, and -RESET goes low with no delay.

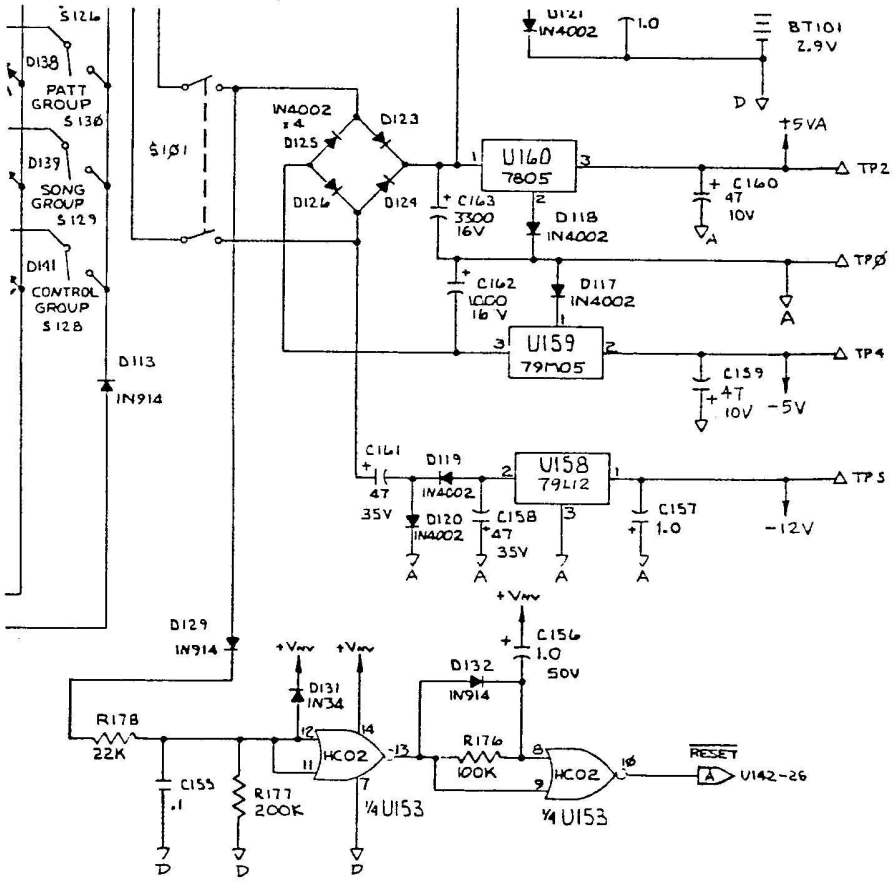


Figure 0.3
ORIGINAL RESET CIRCUIT

EXPANSION

420s are shipped from the factory with 8K of memory installed. Model 871 Memory Expansion kits increase the note capacity of the 420 in 8K (2,700-note) increments to a maximum 32K (10,400 notes). 420's equipped with TOM1_0 - 1_3 software must be updated to at least TOM1_4 status (with Sequential part# Z-1063 software update) to work with the expanded memory. Model 871 Memory Expansion kits are available to service centers or users, and if correctly installed, the 420's one-year limited warranty is not voided.

Users should be aware that expanding the TOM's memory affects its operation with the Model 900A Dumptraks software. The Model 900A can save only 2,350 notes of pattern and song data in one save operation. When the TOM's memory is expanded to 16K, 24, or 32K, there is not sufficient memory in the Commodore 64 computer to hold the additional data.

MECHANICAL DISASSEMBLY/REASSEMBLY

Switch power off before detaching the power cord.

Disconnect the power transformer from the outlet.

Remove the top two screws from each side panel.

Remove the three back panel screws.

Place the 420 face-down on a smooth surface. Be careful not to scratch the front panel.

Remove the three screws from the 420's front lower lip.

To remove the bottom panel, hold onto the side panels, then lift from the back of the 420, away from under the lower lip.
This exposes the 420's PCB.

To gain access to components on the panel-side of the PCB, remove knob from the **MASTER VOLUME** pot, remove the ten PCB screws and washers, then lift the PCB from the front edge so the back panel jacks do not catch the back panel.
It is ok to test the 420 outside of its chassis.

Reconnect power transformer to the 420, then to the outlet.

Before replacing any components, make sure that power is switched off. To solder, use only grounded soldering irons, unless the 420 is disconnected from all other equipment.

Test the 420 for correct operation.

To reassemble the 420, reverse the order of disassembly. (If the PCB was removed, check that all washers are back in place.)

FUNCTIONAL DESCRIPTION

The 420 can be divided into two sub-systems: 1) the main operating system, which determines how and when instrument sounds are played; and 2) the sound-generating system, which converts digitally-encoded sounds from sound memory into four audio signals which are selectively filtered, then panned left, right, or center as determined by the main operating system. Referring to the schematics, these two sub-systems share the main address and data busses, but operate independently to some degree with the aid of U143, the "wonder chip" custom IC, which addresses sound memory using the "sound address" buss.

Main Operating System

The Z-80 is driven by a 4-MHz clock U135/36, which also drives the UART and wonder chip.

U151/U201 memory chip decoders provide "chip selects" for U144 operating ROM, U145/46/47/48 non-volatile RAM, and U141 MIDI UART. When each chip select goes true, the corresponding memory chip can be written to, or read from, as determined by -RD and -WR.

Simiarly, U137/38 I/O Chip Decoder selects the I/O circuits. Switches and LEDs are arranged in matrices. U133/49 latches provide signals for the metronome, tape, clock, and trigger outputs, as well as the CPU interrupt inputs.

Sound-Generating System

The 420's on-board percussion sounds are stored in U155/56, two sound ROMs, while P101 provides the required signals to address optional 260-series sound cartridges.

U143 wonder chip is clocked at 4 MHz, and I/O-decoded by U137. Its internal registers are addressed by Main Address lines MA3-MA5, then filled with instrument event data. U143 then reads sound address data onto the Sound Address Buss, and sound data is read from sound memory onto the Sound Data Buss. U122/25 sound decoding DAC converts eight-bit words into an analog voltage which is demultiplexed by U121/23/24 into four discrete audio channels. Driven by the wonder chip, U120/22 produces a reference voltage which dynamically scales the DAC output, hence, the instrument volumes.

see also page 1.13 and 1.14

So the CPU can properly address and route sound data, U154 "format" latch responds to the state of the LEFT/PHONES jack, the presence of a sound cartridge at P101, and the data format of sound memory.

Each audio channel is followed by filter switching and panning circuits, which are controlled by latches U126/09/04/05, producing left and right audio signals, to which is added the metronome signal before the U101 output buffers.

HARDWARE DESCRIPTION

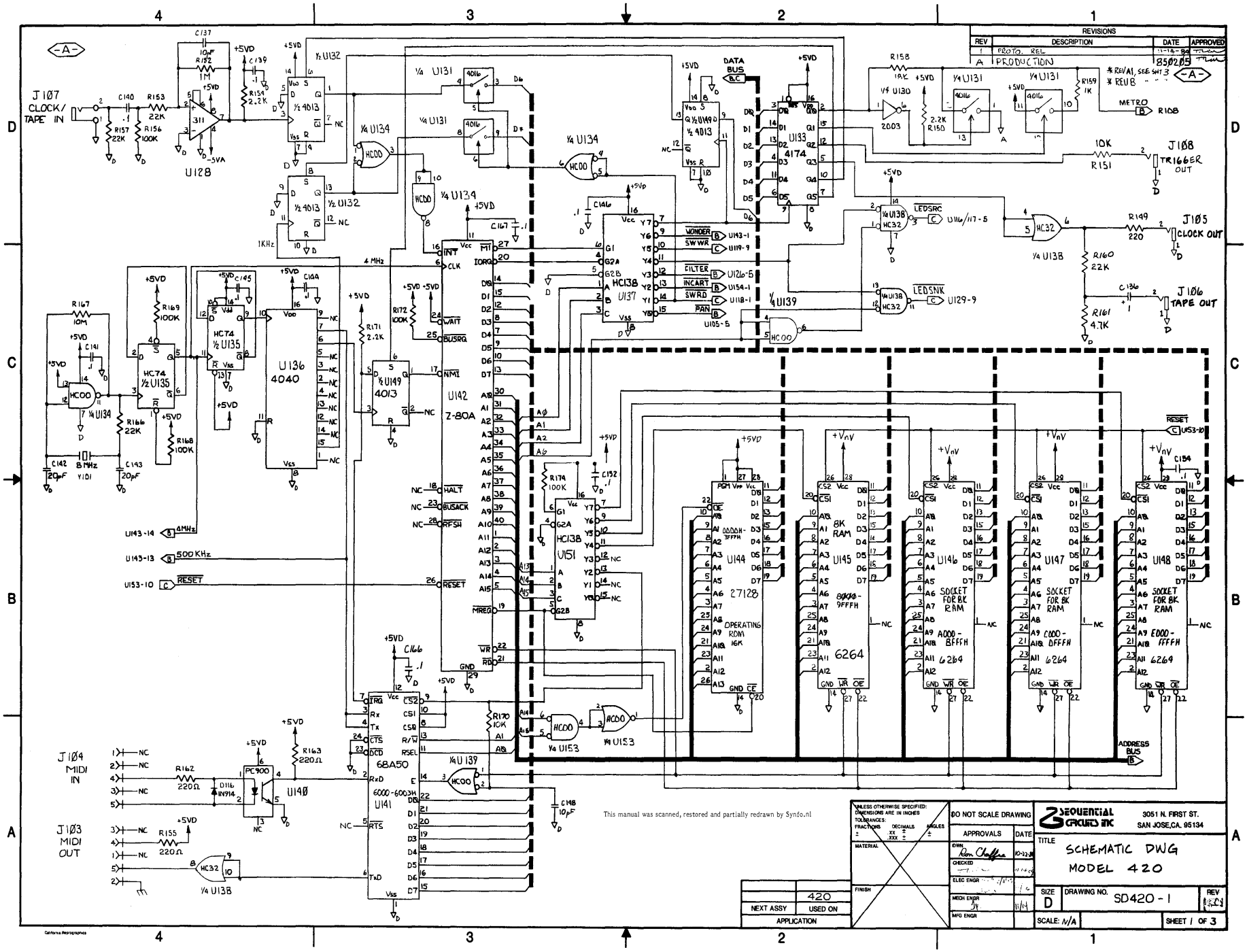
DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION
T2	(110V models)	E-170	15VAC wall-mount transformer
	(220V models)	E-175	

Non-Designated Components

CM420	Operation Manual
CN420-1	Controls and Indicators
CN420-2	Reference Card
CN420-3	Transformer Note
CN420-4	Addendum to MIDIGUIDE
MG420	MIDIGUIDE
MIDI-4	MIDI Control Summary
M-016	large rubber feet
M-026	#6 5/8" black pan hd phil
M-035	6-32 nuts ¼" outside dia
M-071	6-32 X ¼" pan hd phil ms
M-099	4-40 nut ¼" outside dia
M-140	3 ½" tie wrap
M-209	#6 X 3/8" blk pan hd phil
M-357	black knob .250 X .156
M-428	4-40 X ½" pan hd phil
M-501	red acetate window
M-509	1/8 X 3/8 alum pop rivet
MW0420-1	top panel
MW0420-2	bottom panel
PW0420-1	plastic left side
PW0420-2	plastic right side

SECTION 1

PCBS 1 AND 2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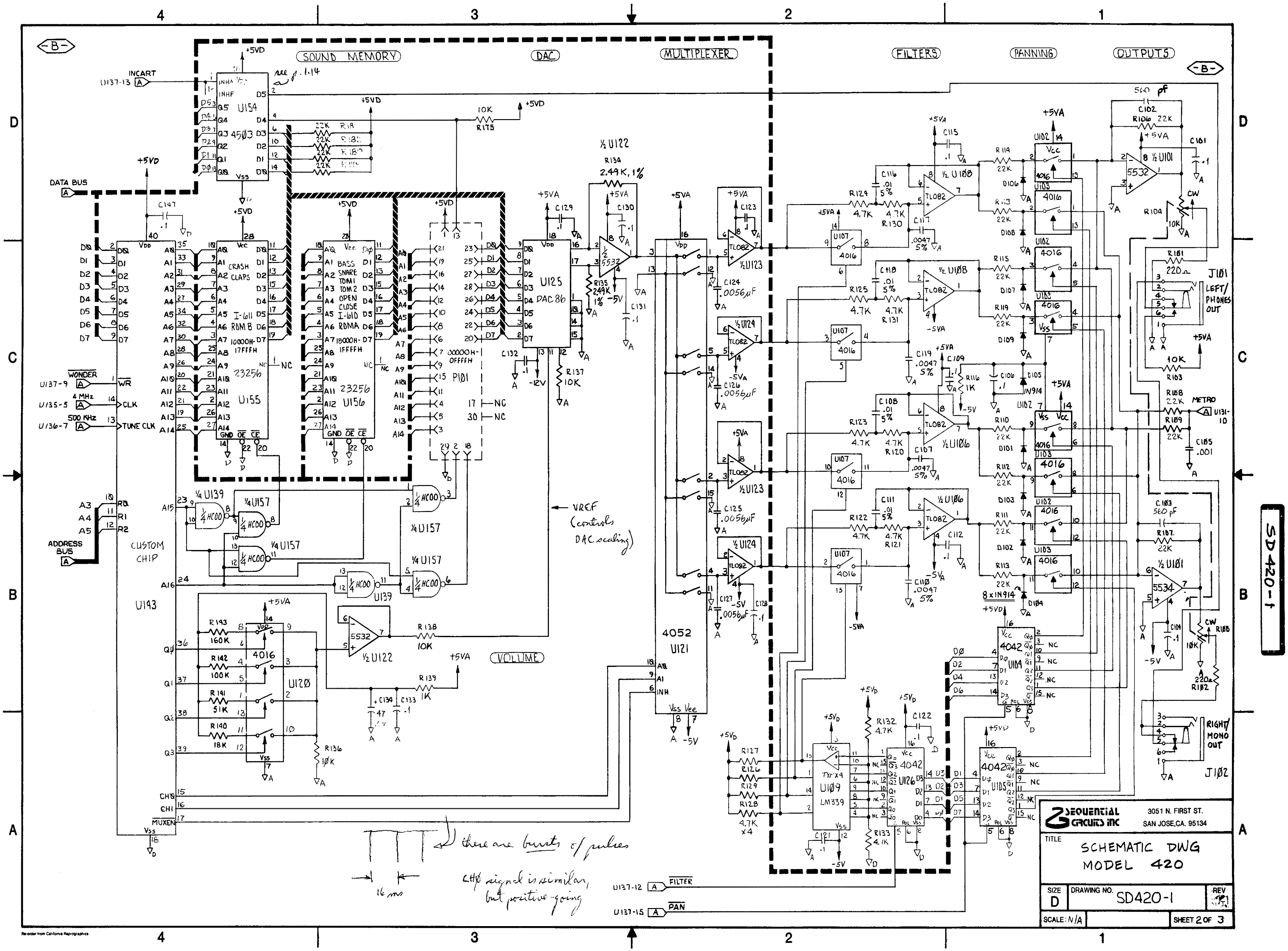
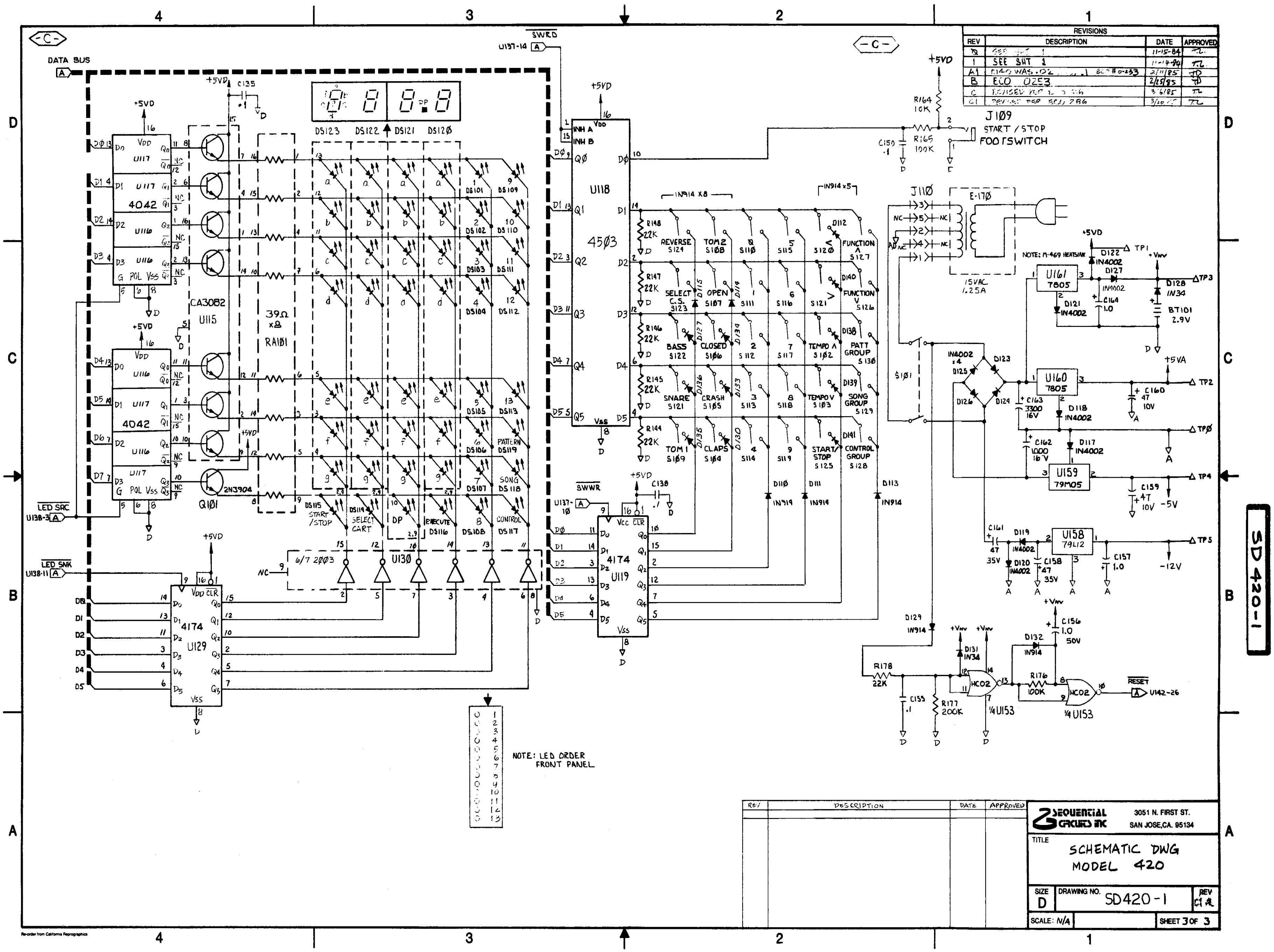
A PRODUCTION 850285
* REV A1, SEE SHT 3
* REV B
J107 CLOCK/ TAPE IN
U128
J104 MIDI IN
J103 MIDI OUT
J108 TR166ER OUT
J105 CLOCK OUT
J106 TAPE OUT
METRO R108
DATA BUS
ADDRESS BUS
U133 4174
U136 4040
U137 HCI38
U141 68A50
U142 Z-80A
U144 27128 OPERATING ROM 16K
U145 8K RAM 6264
U146 SOCKET FOR 8K RAM
U147 SOCKET FOR 8K RAM
U148 SOCKET FOR 8K RAM
U151 HCI38
Y1D1 8 MHz
WONDER
SWWR
FILTER
INCART
SWRD
PAN
LEDSRC
LEDSNK
RESET
4 MHz
500 KHz
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES
TOLERANCES: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DRAWING
APPROVALS DATE
DWN Ron Chaffee 10-22-84
CHECKED
ELEC ENGR
MECH ENGR
MFG ENGR
SEQUENTIAL CIRCUITS INC. 3051 N. FIRST ST. SAN JOSE, CA. 95134
TITLE SCHEMATIC DWG MODEL 420
SIZE D DRAWING NO. SD420-1 REV
SCALE: N/A SHEET 1 OF 3
420 NEXT ASSY USED ON APPLICATION
This manual was scanned, restored and partially redrawn by Synfo.nl
SD420-1


SOUND MEMORY
DAC
MULTIPLEXER
FILTERS
PANNING
OUTPUTS
INCART
DATA BUS
ADDRESS BUS
CUSTOM CHIP
U143
U154 4503
U155 23256 I-611 ROM B 10000H-17FFFH
CRASH CLAPS
U156 23256 I-610 ROM A 18000H-1FFFFH
BASS SNARE TOM1 TOM2 OPEN CLOSE
P101 00000H-0FFFFH
U125 DAC 86
1/2 U122 5532
4052 U121
VREF (controls DAC scaling)
VOLUME
4016 U120
U109 LM339
U126 4042
U104 4042
U105 4042
8 x IN914
J101 LEFT/PHONES OUT
J102 RIGHT/MONO OUT
METRO
FILTER
PAN
there are bursts of pulses
CH0 signal is similar, but positive-going
16 ms
SEQUENTIAL CIRCUITS INC
3051 N. FIRST ST.
SAN JOSE, CA. 95134
TITLE
SCHEMATIC DWG
MODEL 420
SIZE D
DRAWING NO. SD420-1
SCALE: N/A
SHEET 2 OF 3
SD420-1
Re-order from California Reprographics


REVISIONS
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A1 C140 WAS .02 2/11/85
B ECO 0253 2/25/85
DATA BUS
LED SRC
LED SNK
SWRD
SWWR
CA3082 U115
39Ω x8 RA101
4042
4503
U118
4174
U119
U129
U130
J109 START / STOP FOOTSWITCH
J110
E-170
15VAC 1.25A
REVERSE S124
TOM2 S108
SELECT C.S. S123
OPEN S107
BASS S122
CLOSED S106
SNARE S121
CRASH S105
TOM 1 S109
CLAPS S104
FUNCTION S127
FUNCTION S126
PATT GROUP S130
SONG GROUP S129
CONTROL GROUP S128
TEMPO S102
TEMPO S103
START/ STOP S125
U161 7805
U160 7805
U159 79M05
U158 79L12
BT101 2.9V
NOTE: M-469 HEATSINK
HC02 ¼ U153
RESET U142-26
NOTE: LED ORDER FRONT PANEL
SEQUENTIAL CIRCUITS INC
3051 N. FIRST ST.
SAN JOSE, CA. 95134
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MODEL 420
SIZE D
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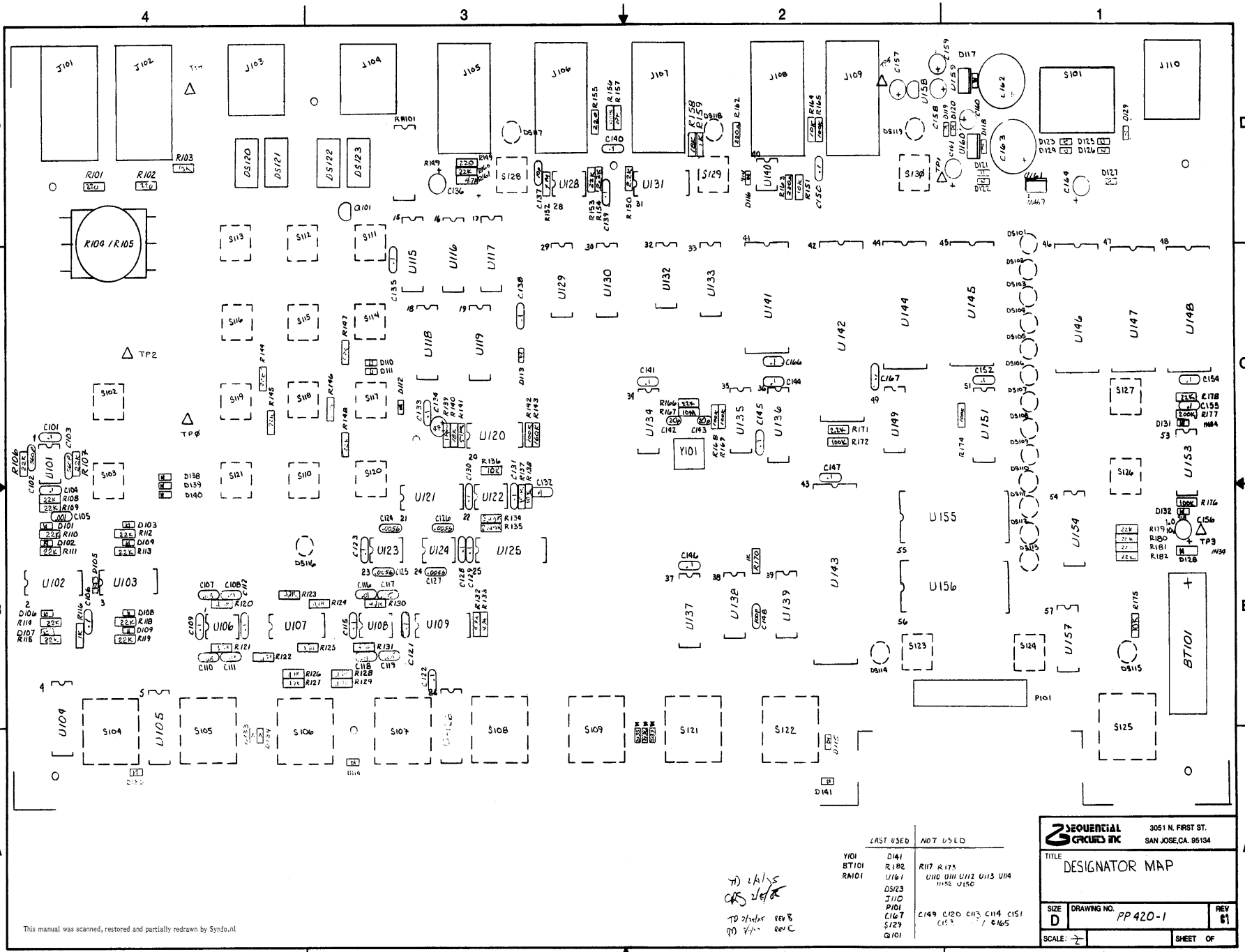
SHEET 3 OF 3
SD 420-1



PP420-1

LAST USED		NOT USED
Y101	D141	
BT101	R182	R117 R173
RN101	U161	U110 U111 U112 U113 U114 U155 U150
	DS123	
	J110	
	P101	
	C167	C149 C120 C113 C114 C151 C153 / C165
	S129	
	Q101	

TD 2/21/85 REV B
RD 7/--/-- REV C

SEQUENTIAL CIRCUITS INC. 3051 N. FIRST ST. SAN JOSE,CA. 95134

TITLE: DESIGNATOR MAP

SIZE D | DRAWING NO. PP420-1 | REV 61

SCALE: 1/2 | SHEET OF

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION

Integrated Circuits

U101 **Audio Summers** I-324 5532 dual op-amp

Pin 1 produces the left audio output from U102-1, -4, -8, and -10, and the metronome signal from U131-10. Pin 7 produces the right audio output from U103-1, -4, -8, and -10, and the metronome signal from U131-10. Volume of each output is attenuated by R104/05.

U102/03 **Panning switches** I-206 4016 quad analog switch

Outputs from U102 feed U101-2, left audio summer. Outputs from U103 feed U101-6, right audio summer. Control inputs -13, -5, -6, and -12 (from U104) determine whether or not signals present at -2, -3, -9, and -11 are switched to their respective outputs.

Diodes D101-04, and D106-09 prevent the inputs from going lower than -0.6V. R116/C106/D105 provide -0.6V negative bias for protection in this worst case condition.

U104/05 **Pan Control Latches** I-227 4042 quad latch

Outputs -2, -10, -11, and -1 control the panning of the four audio channels. A high output from U104 allows U102 to switch the corresponding audio channel through to the left audio summer. A high output from U105 allows U103 to switch the corresponding audio channel through to the right audio summer. -PAN enable, which latches stereo selection data, comes from U137-15.

U106 **Channel 3/4 Filter** I-312 TL082 bifet op-amp

To reduce high frequency content of specific sounds, pins -7 and -1 selectively filter audio channels 3 and 4 (from U123-1 and U124-1 respectively) when the demultiplexer has assigned that sound to these channels. Switches U107-1 and -11 determine whether U106 acts as a 2-pole filter (switch open) or unity-gain buffer (switch closed).

U107 **Filter Switches** I-206 quad 4016 analog switch

Determine effect of U106 and U108 channel filters. When switch is open (negative input at -6, -5, -12, or -13), the corresponding audio channel is passed through a 2-pole filter. When switch is closed (positive control input), the audio signal appearing at -9, -3, -10, and -2 is switched through to -8, -4, -11, and -1 (respectively), bypassing the RC network, making the op amp behave as a unity-gain buffer.

Power supplies are +/-5V, allowing 10-V peak-to-peak signals to pass. Control inputs (from U109) for each switch are +5V to close, and -5V to open the switch.

U108 **Channel 1/2 Filter** I-312 TL082 bifet op-amp

Operates similarly to U106, selectively filtering channels 1 and 2. Switches U107-8 and -4 determine whether U108 acts as a 2-pole filter or unity-gain buffer.

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION

U109 — **Level Converter** — **I-302** — **LM339 quad comparator**

Converts 0-5V signals from U126 into +/-5V signals required to control U107 filter switches. Switching thresholds are set at +2.5V by R132/33 so that a 0-V input causes a -5V output (at -13, -1, -14, and -2), and a +5V input causes a +5V output. Resistors R126-29 pull up U109's open-collector outputs.

U110-U114 — **NOT USED**

U115 — **LED Matrix Drivers** — **T-011** — **CA3082 transistor pack**

When switched on by U116/17, connect LED anodes to +5V. Q101 handles the remaining row of LEDs.

U116/17 — **LED Driver Latches** — **I-227** — **4042 quad latch**

U116 and U117 together latch the eight rows of LED information from the data buss. U116 latches bits D_2, D_3, D_4, and D_6, while U117 latches bits D_0, D_1, D_5, and D_7. The latching is accomplished on command of -LEDSRC, from U138-3, a decoded Z-80 I/O write signal. A high is present on the data buss at this time for each LED to be lit in the currently active column (see U129 and U130). This high is buffered by LED drivers Q101 (for D7) and U115 (for the others), current limited by a 39 ohm resistor in RA101, and applied to the anodes of the LEDs in the row. One of the columns is active, with a low on one output of U130. With this low applied to the cathode of the LED and a high on the anode, the LED lights. This column only stays lit for a few milliseconds, then the processor targets the next column, continually multiplexing the LEDs.

U118 — **Switch Input Buffer** — **I-216** — **4503 hex tri-state buffer**

The 4503's two sections are combined (pin 1 tied to pin 15) to gate information from the switch array on to the data buss. The input command from the CPU is decoded by U137-14 and applied to U118 as -SWRD.

One of the seven columns of the switch array having been set high by U119, the high propagates through any closed switch on the row, overriding the low normally kept on the input by one of the pull-down resistors R144-48. The pattern of switches for that column, then, is placed on the data buss when -SWRD goes low.

U118 also serves as the footswitch input. The footswitch line is normally pulled up by R164. When the footswitch is connected and closed, the falling transition is smoothed by R165 and C150.

U119 — **Switch Driver** — **I-228** — **4174 hex latch**

When strobed by -SWWR (from U137-10), data buss lines D0-D5 select the output bit (Q0-Q6) which is to go high, the remainder go low. This high output activates one of the columns of the switch matrix. If a switch is closed, the high is coupled to the corresponding pin of U118. D112, D130, and D133-41 prevent the outputs of U119 from being connected to each other when common combinations of switch

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION

U119 (continued)

closures occur. D110, D111, and D113-15 protect the outputs of U119 when less common switch combinations occur.

U120 **Switching Attenuator** I-206 **4016 quad analog switch**

Attenuates +5VA supply (filtered by R139 and C133/34 for clean dc) by switching current through weighted resistors R140-43, creating a digital potentiometer with R136. The gate of each section of U120 comes from Q0-Q3 (U143, pins 36-39). With all gates low, U122-5 (DAC Reference Buffer) is pulled down to 0V by R136. With all gates high, the parallel resistor network impedence is approximately 11K, and U122-7 reaches its peak of 2.4V.

U121 **Channel Demultiplexer** I-277 **4052 multiplexer**

Decodes four independent audio signals from the multiplexed VDAC signal. When -MUXEN (at pin -6) goes low, CH0 and CH1 (U143-15 and -16) select the channel sample/hold (U123/24) to which VDAC (at U121-3) is routed.

+/-5V supplies allow switching of ac-coupled signals. One half of the chip is used.

U122-1 **DAC Output Balanced Amplifier** I-324 5532 dual op amp

Converts U125 DAC's current outputs (pins -16 and -17) into ac voltage VDAC, which is decoded by U121 Channel Demultiplexer, then fed to sample/holds U123 and U124.

U122-5 **DAC Reference Buffer** I-324 5532 dual op-amp

See U120 Switching Attenuator.

U123/24 **Sample/Holds** I-312 **TL082 bifet op-amp**

Each sample/hold consists of a .0056uF cap followed by a unity-gain buffer. Before the Wonder Chip addresses the next byte of sound memory for conversion, -MUXEN goes high, disabling the DMUX. The S/H cap, having no discharge path through the high impedence input of the op amp, holds the last value of VDAC until it is strobed again.

U125 **8-Bit Companding DAC** I-515 **DAC86 companding DAC**

Generates multiplexed audio by converting bytes appearing on the Sound Data Buss. Current outputs -16 and -17 are sensed by U122 DAC Output Amplifier to produce VDAC at U122-1. For each byte of sound memory converted, the Wonder Chip generates four volume control bits (Q0-Q3), which are converted into an analog voltage (Vref) by U120 Switching Attenuator. U122-7 buffers this volume control voltage, which R138 converts to current suitable for driving U125-11. Adjusting the reference in this way gives direct control of the maximum DAC voltage.

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION
U126	Filter Latch	I-227	4042 quad latch

Generates control signals for U107 filter switches. When pin -5 is strobed low by -FILTER (from U137-12), D0-D3 are latched at outputs Q0-Q3. U109 converts these outputs to +/-5V levels to drive U107. Pin -6 is tied to ground to set the polarity of the strobe.

U128	Clock Comparator	I-301	311 precision comparator

Converts ac-coupled data from tape, or dc-coupled pulses from other clock sources into pulses which are polled by the interrupt detect circuitry (see U131, U132). With no input, R156/R183/R153 provide negative bias to the non-inverting input (pin 2), keeping output pin 7 low. When positive input is sensed, R154 pulls the open-collector output high, while R152/C137 ensure output switches state quickly and smoothly. (Earlier units may require that R183 be added.)

U129	LED Sink Latch	I-228	4174 hex latch

Latches the LED sink data from the data buss when strobed by I/O chip select -LED SNK (from U138-11). The currently-active output is high, the rest are low.

U130-15, -12, -10, -14, -13, -11	LED Matrix Sink	I-235	MC1413 (2003) hex driver

Inverts the signal from LED sink latch U129, and sinks LED current. Only one output should be active (low) at a time.

U130-16	Metronome Gate Inverter	I-235	MC1413 (2003) hex driver

When low level from U133-2 is present at pin 1, R150 pulls the open-collector output pin 16 high.

U131-3, -9	Interrupt Buffers	I-206	4016 quad analog switch

Allow the CPU to determine the source of the interrupt detected by U134-3. Normally, when I/O chip select -SWRD (U137-14) goes low, D0-D5 (from U118) carry switch matrix information while D6 and D7 (U131-3 and -9) are ignored. When an interrupt is detected (see U132) -SWRD goes low and the CPU checks D6 and D7 to determine if the interrupt comes from U128 clock/tape comparator or the 1 msec interrupt pulse generated by U136-15. U134-6 inverts -SWRD to produce the required positive gates at U131-5 and -6.

U131-2, 10	Metronome Switches	I-206	4016 quad analog switch

Creates 1 msec pulses to feed the audio outputs. Outputs Q0 and Q1 from U132-2 and-15 combine to select one of three metronome signal (METRO) levels (off, normal, or accent). When both Q0 and Q1 are low, the low level at pin 12 leaves R159 floating, while the high level at U131-13 (inverted by U130-16) shorts pins 1 and 2, grounding METRO. For a normal metronome pulse, Q0 is high for 1 msec, removing the ground from U131-2, and current flows through R158. For a louder metronome, Q1 also goes high. This shorts U131-11 and -10, and current through R158 is summed with current which now flows through R159.

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION
U132-1, -13	Interrupt Latch	I-205	4013 dual flip-flop

When pin 6 is strobed by U133-10, pin 1 is set high. Since pin 5 is grounded, when a positive edge from U128 clock comparator appears at pin 3, pin -1 goes low. Similarly, a strobe from U149-13 sets U132-13 until a pulse from U136-15 (every 1 msec) clocks the low level at U132-9 through to pin 13.

U134-3 senses either of these low outputs. U134-8 inverts to produce a low strobe at the CPU's maskable interrupt input. The CPU then reads U131-3 and -9 interrupt buffers to determine whether the interrupt comes from the clock comparator or clock divider.

U133 — Misc Output Latch — I-228 — 4174 hex latch

When strobed by -MISC I/O chip select, reads D0-D5 from the data buss to generate miscellaneous output signals and strobes for U132 and U149 interrupt latches, the metronome, trigger, tape, and clock outputs. U133-5 is inverted at U138-6 to generate the Clock Out and Tape Out signals.

U134 — Misc NAND Gates — I-264 — 74HC00 quad NAND gate

(See U131, U132, and U135)

U135 — Clock Dividers — I-252 — 74HC74 dual latch

Both sections are similarly configured to divide the 8 MHz clock from U134-11 to 4 MHz, then again to 2 MHz. U135-5 drives U142 Z-80A and U143 Wonder chip, while -9 drives U136 clock divider. R168/69 allow pins 1 and 4 to be pulled low for factory testing.

U136 — Clock Divider — I-272 — 4040 counter

Divides the 2 MHz clock at pin 10 (from U135-9) to 500 kHz, 250 kHz, and 1 kHz. These outputs drive (respectively) U141 ACIA and U143 Wonder chip, U149 NMI latch, and U132 interrupt latch.

U137 — I/O Chip Decoder — I-253 — 74HC138

Generates I/O chip selects. Outputs are normally high. When -MI (from U142-27) is high, and IORQ (U142-20) is low, A0-A2 (to pins -1, -2, and -3) determine which of the chip selects goes low. These chip selects allow the CPU to monitor the switch matrix and other internal signals or generate miscellaneous output signals. The -M1 signal is present to prevent a chip select during the interrupt acknowledge cycle of the CPU.

U138-3 and -11 — Misc OR Gates — I-251 — 74HC32 quad OR gate

Combine the chip select from U137-11 with A6 to generate -LEDSRC and -LEDSNK. When A6 is low, -LEDSRC goes low. When A6 is high, -LEDSNK goes low. (A6 is inverted at U139-6 to drive U138-1.)

U138-6 — Misc OR Gates — I-251 — 74HC32 quad OR gate

Inverts the Clock Out signal from U133-5. R160/61 attenuate the Clock Out signal to a suitable level for tape inputs.

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION
U138-8	Misc OR Gate	I-251	74HC32 quad OR gate

Inverts the MIDI OUT signal from U141-6.

U139-8 and -11	Misc NAND Gates	I-264	74HC00 quad NAND gate

In the Sound Memory decoding circuit, invert SA15 and SA16 (from U143).

U139	Misc NAND Gate	I-264	74HC00 quad NAND gate

(See U138 and U141.)

U140	Optoisolator	I-330	PC900 optoisolator

The current from a MIDI transmitter similar to U138-8 (described under U141) comes in pin 5 of J104, through pin -2, the internal LED, through pin -1 and R162, and out J104-4. Current through the LED turns it on, and its light turns on the adjacent phototransistor (between pins 4 and 5), which places a low on U141-2, RXDATA. If no current is flowing, R163 pulls RXDATA high.

U141	ACIA	I-066	68A50 UART

U141 Asynchronous Communications Interface Adaptor (ACIA) converts parallel data from the CPU into serial form for transmission over MIDI, and transfers received MIDI data to the CPU.

The CPU communicates with the ACIA by means of the data buss, various address lines, the -WR line, and the chip select from U151 memory address decoder. To write or read, the CPU sets -CS2 (pin 9) low, by addressing any location between 4000H and 4003H. To read, address A1, going to R/-W, is set high; it is low to write. RSEL (A0) selects the ACIA internal register. Once the address and data lines are steady, the actual data transfer occurs on the falling edge of 'E' (pin -14).

Once a byte to be transmitted has been placed in the ACIA, it is shifted out TXDATA, bit by bit, one bit for every 16 TX clock pulses (pin 4). The TX clock is supplied by 500 kHz from U136-7, and divided to the 31.25 kBaud MIDI transmission rate. When the TXDATA output is low, U138-8 is low, and since R155 pulls J103-4 high, current flows through the external MIDI circuit. If TXDATA is high, no current flows.

Incoming MIDI data is converted from a current loop in the MIDI cable to a logic signal by U140 optoisolator, and applied to RXDATA of the ACIA. This data stream is converted to parallel form by referring it to the RX clock (pin 3).

After a byte is completely received or completely transmitted, -IRQ (pin 7) goes true, requesting non-maskable interrupt service from the CPU via U149-1.

Since RS-232 protocols are not applicable, -RTS, -CTS, and -DCD are not used.

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION
U142	CPU	I-058	Z-80A microprocessor

The Z-80A microprocessor unit (CPU) runs on a 4 MHz clock from U135-5. At power on, the CPU's -RESET input (from U201-8) goes high, causing the CPU to begin execution at ROM location 0. The CPU places the address of a memory or I/O location on the address buss (A0-A15) and activates control signals -IOREQ, -MREQ, -RD, and -WR to command external devices to either place data on the data buss (D0-D7) or take it off. -M1 is used to protect against spurious I/O chip selects during the Z-80A interrupt acknowledge cycle (see U137). -BUSAK, -HALT, -RFRSH, and -WAIT are not used. -BUSRQ is used only for factory testing, so it is pulled up with R172.

Interrupt inputs -INT and -NMI are important signals in the system. -INT (from U134-8) has two possible sources: the clock/tape interrupt from U132-1, and the regular 1 msec interrupt from U132-13. When answering an interrupt, the CPU polls the -MISC interrupt buffers (see U131-3 and -9) to determine where the interrupt came from. The 1 msec interrupt from U136-15 (via U132-13) is used to update the LEDs, read switches, and as a timebase for patterns and other internal counters.

-NMI is normally high because strobes from U133-7 set U149-1. Pulses every 4 usec at pin 3 (from U136-6) strobe the level at pin 5 through to pin 1. When the ACIA is inactive, R171 pulls U149-5 high. When U141 ACIA receives a byte from MIDI, or finishes transmitting one, -IRQ goes low, and upon the next clock at U149-3, -NMI is true.

U143	Wonder Chip	I-607	Custom IC

Receives event data from the CPU to coordinate the conversion of sound memory into four raw audio signals. This leaves the CPU with the less demanding tasks of filtering and panning the signals.

When an instrument event occurs (in pattern playback, or live playing), the CPU selects U143 with -WONDER (from U137-9) and loads the chip's internal registers with details of the event (pitch, volume, direction, channel number, starting address, and length). U143 then generates the signals required to generate the event, independent of the main operating system.

U121 channel demultiplexer is normally disabled with a high level from -MUXEN (pin -17). The Wonder Chip (WC) then writes an address onto the Sound Address Buss, and sound data is read from ROMs A-D (decoded by U139-8, U139-11, and U157) onto the Sound Data Buss, which feeds U125 8-bit DAC. Q0-Q3 (pins 36-39) control U120 to produce a variable VREF, which determines the volume of each event by scaling the DAC.

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION

U143 (continued) — **Wonder Chip** — I-607 — custom chip

When the sound memory and DAC settle, pins 15 and 16 select one of the four channel sample/holds (U123 and U124) with CH0 and CH1. To route VDAC to the selected sample/hold, -MUXEN goes low, enabling U121. After a short period, -MUXEN goes high, disabling U121. The WC then prepares to convert the next byte of sound data.

Before generating the address of the next byte to be converted, the WC waits a period inversely proportional to the pitch at which the sound is to be played, using the 500 KHz clock input as a timebase. U143-14 receives a 4 MHz clock from U135-5 generate accurate internal timing signals.

If several sounds are playing concurrently (four maximum), the WC looks to see which sound needs to be addressed next. If the next sound to be addressed is the not the same as the last, the WC selects the required channel S/H, rescales the DAC with Q0-Q3, then generates the next address for that sound before re-enabling the channel demultiplexer.

As the sounds in memory may change due to the cartridge port, to maintain a list of the starting address and length of all sounds currently in memory, on power-on, and when a cartridge is inserted, the CPU selects U154 status buffer to read "headers" from each ROM.

U144 — **Model 420 Firmware Version TOM1_5** — Z-1063 — 27128 firmware ROM

Contains the operating software for the CPU. Address and data busses are connected to the CPU, and the CPU reads the ROM by making -MREQ low, then decode/activate -OE, pin -22, addressing 0000H-3FFFH.

U145-U148 — **Non-volatile RAM** — I-071 — 6264 8K X 8 static RAM

These RAMs provide scratchpad storage and non-volatile pattern and song storage for the Z-80A. To either read (-OE) or write (-WE), the chip select must be enabled with U151 memory chip decoder. Supply from Vnv allows the 420 to retain its memory when power is switched off. (When power is off, -RESET (at CS2, pin 26) is low to prevent accidental memory loss.)

Model 420s are shipped from the factory with only U145 installed. Optional 8K RAM chips are available as Model 871 Memory Expansion kits, allowing expansion to 32K of RAM.

U149-1 — **-NMI Latch** — I-205 — 4013 dual flip-flop

(See U142.)

U149-13 — **Misc Latch Section** — I-205 — 4013 dual flip-flop

When enabled by -MISC, latches D6 from the data buss to strobe U132-8 interrupt latch, setting U132-13.

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION

U150 Not Used

U151 **Memory Chip Decoder** I-253 74HC138

When enabled by -MREQ, A13-A15 (at pins 1-3) are decoded to enable one of eight memory blocks. G1 is pulled high by R174, allowing it to be pulled low for factory testing.

U152 Not Used

U153 **Not Used in serial numbers 1882 and above.**
(For details on earlier models, see Memory Loss, page 0.1.)

U154 **Status Buffer** I-216 4503 tri-state buffer

When selected with -INCART (from U137-13), the CPU checks the status of the output jacks, and the cartridge port. When nothing is plugged into the LEFT/PHONES jack, J101-5 is grounded, and all audio is panned to the right output for monophonic operation. When the LEFT/PHONES jack is used, pin 5 is pulled high by R103, and audio signals are panned left or right as required.

Similarly, R175 pulls D4 high, unless a cartridge is plugged into P101, in which case D4 is grounded by P101-13. When the CPU detects a change in status of the cartridge port, it reads the "headers" of each sound ROM to determine the addresses and lengths of sounds currently in memory. To do this, U143 wonder chip addresses sound memory, and this buffer places the "headers" in four-bit nibbles from the Sound Data Buss (SD0-SD3) on the Main Data Buss.

U155 **Sound ROM B** I-611 23256 masked ROM-B

All sounds are stored in ROMs. Each sound has a starting address, a length, and a filtering status. Sound memory has its own address and data buss, so that it can operate independently of the main operating system.

The factory sounds are stored on ROMs A and B, while additional sound memory is from optional 260-series sound cartridges. Sound memory is decoded by U157, U139-8, and U139-11. Sound data is stored in consecutive addresses, beginning with the starting address. For each address appearing on the Sound Address Buss, a byte of sound data is read onto the Sound Data Buss, which is then converted into an analog voltage (VDAC) by the DAC.

To recreate a sound waveform, the sound's addresses are read through at a rate determined by the event pitch. The higher the pitch, the faster the sound address counter is incremented. To create the effect of a reversed sound, the last address is generated first, then decremented for the next byte.

U156 **Sound ROM A** I-610 23256 masked ROM-A

See U155.

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION
U157	Sound ROM Decoder	I-264	74HC00 quad NAND gate
	Generate chip selects from sound address lines SA15 and SA16 (inverted by U139-8 and -11). Low levels at U157-8 and -11 select sound ROMs B and A (respectively), while U157-3 and -6 select sound ROMs on optional 260 series sound cartridges.		
U158	-12V Regulator	I-431	79L12 -12V reglator
	Powers U125 DAC.		
U159	-5V Regulator	I-411	LM7905/79MO5 -5V reg
	Powers analog circuits. D117 causes the regulator to produce -5.6V, allowing analog circuits to handle the 5-V signals produced in the digital circuits.		
U160	+5V Regulator	I-410	7805 +5V regulator
	U160 powers analog circuits. D118 increases the regulator's output to +5.6V.		
U161	+5V Regulator	I-410	7805 +5V regulator
	Powers the digital circuits. D121 raises the regulated output to +5.6V. D122 supplies digital circuits. D127 blocks Vnv from being drained by everything else, but at power-on allows +5V to override Vnv to provide full operating voltage to RAMs. D128 prevents +5V from charging BT101. Vnv yields 2.3 --enough for static memory retention.		
U201-3, -6	Operating ROM Decoder	I-289	74HC132 quad NAND gate
	Since U144 firmware ROM represents a 16K block of memory, it is decoded differently from the 8K memory blocks. U151-14 and -15 go to U201-1 and -2 via TB201-1 and -2 jumper wires. When U151-14 or -15 go low, U201-3 goes high. This level is inverted at U201-6, which enables U144.		
U201-8, -11	Power Detect	I-289	74HC132 quad NAND gate
	Power is supplied to U201 by Vnv at pin -14. When power is off, D131 is reverse-biased, pin -12 is brought low by R177, bringing pin -11 high, and pin -8 is held at Vnv by C156, ensuring that -RESET is low at power-up. When power is switched on, D129/R178/C155 generate unregulated dc at pin -12, bringing pin -11 low. D132 is reverse-biased, and R176/C156 delay the falling edge at pins -9 and -10, followed by -RESET (pin -8) going high. On power-off, pin -11 goes high, forward-biased D132 bypasses R176, and -RESET goes low with no delay.		

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION
Other Components			
BT101	Non-volatile Memory Supply	E-040	2.9V lithium battery
C101		C-045	.1 uF 50V mono radial
C102/03		C-007	560 pF
C104		C-045	.1 uF 50V mono radial
C105		C-008	.001 50V 10% mylar radial
C106		C-045	.1 uF 50V mono radial
C107		C-099	.0047 50V mylar radial
C108		C-102	.01 50V 5% mylar radial
C109		C-045	.1 uF 50V mono radial
C110		C-099	.0047 50V mylar radial
C111		C-102	.01 50V 5% mylar radial
C112		C-045	.1 uF 50V mono radial
C113/14	Not Used.		
C115		C-045	.1 uF 50V mono radial
C116		C-102	.01 50V 5% mylar radial
C117		C-099	.0047 50V mylar radial
C118		C-102	.01 50V 5% mylar radial
C119		C-099	.0047 50V mylar radial
C120	Not Used.		
C121-23		C-045	.1 uF 50V mono radial
C124-27		C-046	.0056 uF
C128-33		C-045	.1 uF 50V mono radial
C134		C-103	47 uF 10V elect radial
C135		C-045	.1 uF 50V mono radial
C136		C-080	1.0 uF 50V elect radial
C137		C-002	10 pF 50V 10% disc radial
C138-41		C-045	.1 uF 50V mono radial
C142/43		C-065	20 pF
C144-47		C-045	.1 uF 50V mono radial
C148		C-002	10 pF 50V 10% disc radial
C149	Not Used.		
C150		C-045	.1 uF 50V mono radial
C151	Not Used.		
C152		C-045	.1 uF 50V mono radial
C153	Not Used.		
C154/55		C-045	.1 uF 50V mono radial
C156/57		C-080	1.0 uF 50V elect radial
C158		C-105	47 uF 35V elect radial
C159/60		C-103	47 uF 10V elect radial
C161		C-105	47 uF 35V elect radial
C162		C-096	1000 uF 16V elect radial
C163		C-075	3300 16V elect radial
C164		C-080	1.0 uF 50V elect radial
C165	Not Used.		
C166/67		C-045	.1 uF 50V mono radial
D10116		D-005	1N914
D117-27		D-001	1N4002

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION
D128		D-008	1N34
D129/30		D-005	1N914
D131		D-008	1N34
D132-41		D-005	1N914
DS10119		L-001	large red LED TI
DS120-23		L-009	7-segment display
J101	**Left/Phones Output**	J-090	½" stereo jack w/swton
J102	**Right/Mono Output**	J-090	½" stereo jack w/swton
J103/04	**MIDI Jacks**	J-087	5-pin pc mount din conn
J105-09	**Misc Jacks**	J-100	¼" mono phone jack
J110	**Power Jack**	J-099	5-pin 240 degree din conn
P101	Cartridge Port	J-101	30-pin female edge conn
Q101		T-002	2N3904 transistor
R101/02		R-003	220 ¼W 5%
R103		R-012	10K ¼W 5%
R104/5		R-246	pot dual gang 100K linear
R10615		R-040	22K ¼W 5%
R116		R-008	1K ¼W 5%
R117	Not Used.		
R118/19		R-040	22K ¼W 5%
R120-33		R-011	4.7K ¼W 5%
R134/35		R-137	2.49K ¼W 1%
R136-38		R-012	10K ¼W 5%
R139		R-008	1K ¼W 5%
R140		R-039	18K ¼W 5%
R141		R-056	51K ¼W 5%
R142		R-025	100K ¼W 5%
R143		R-065	160K ¼W 5%
R144-48		R-040	22K ¼W 5%
R149		R-003	220 ¼W 5%
R150		R-034	2.2K ¼W 5%
R151		R-012	10K ¼W 5%
R152		R-029	1M ¼W 5%
R153		R-040	22K ¼W 5%
R154		R-034	2.2K ¼W 5%
R155		R-003	220 ¼W 5%
R156		R-025	100K ¼W 5%
R157		R-040	22K ¼W 5%
R158		R-039	18K ¼W 5%
R159		R-008	1K ¼W 5%
R160		R-040	22K ¼W 5%
R161		R-011	4.7K ¼W 5%
R162/63		R-003	220 ¼W 5%
R164		R-012	10K ¼W 5%
R165		R-025	100K ¼W 5%
R166		R-040	22K ¼W 5%
R167		R-045	10M ¼W 5%

DESIGNATOR	FUNCTION	SEQUENTIAL PART #	DESCRIPTION
R168/69		R-025	100K ¼W 5%
R170		R-012	10K ¼W 5%
R171		R-034	2.2K ¼W 5%
R172		R-025	100K ¼W 5%
R173	Not Used.		
R174		R-025	100K ¼W 5%
R175		R-012	10K ¼W 5%
R176		R-025	100K ¼W 5%
R177	(Rev C_1 PCBs)	R-026	200K ¼W 5%
R177	(Rev C_2 PCBs)	R-065	160K ¼W 5%
R178-82		R-040	22K ¼W 5%
R183	(kludged over U128)	R-030	2.2M ¼W 5%
	Improves performance of the cassette interface. Serial numbers 001-170 and 351-806 do not have this mod, and should be updated.		
RA101		R-300	39 X 8 resistor network
S101		S-092	pc mount rocker switch
S102/03		S-089	Omron key switch
S104-09		S-069	ECG 13001 switch
S110-21		S-089	Omron key switch
S122		S-069	ECG 13001 switch
S123/24		S-089	Omron key switch
S125		S-069	ECG 13001 switch
S126-30		S-089	Omron key switch
S131		S-069	ECG 13001 switch
	Note: Switch caps listed below.		
TB201-1, -2	Jumper wires from U151 to PCB 2		24 AWG str. wire
Y101		E-112	8 MHz crystal

Non-designated Components

	J-016	40-pin DIP socket
	J-045	28-pin DIP socket
Three unused sockets are provided for memory expansion with Model 871 kits.		
For PCB2.	J-107	14-pin wire wrap socket
For U161.	M-504	short heatsink
	PC-0420-1	blank PCB1
	PC-0420-2	blank PCB2
	S-093	Omron gray switch cap
	S-094	Omron orange switch cap
	S-095	Omron blue switch cap
	Z-350	420 PCB1 assembly
	Z-351	420 PCB2 assembly